REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1-59 are in this case. Claims 20-30 and 50-59 were withdrawn by the Examiner from consideration as drawn to a non-elected invention. Claims 5, 6, 9, 16 and 17 have been rejected under § 112, second paragraph. Claims 1, 4, 5, 7, 9, 10, 12, 14-19, 31, 34, 35, 37, 38, 40, 42 and 44-49 have been rejected under § 102(e). Claims 2, 3, 6, 8, 11, 13, 32, 33, 36, 39, 41 and 43 have been rejected under § 103(a). Dependent claims 2, 13, 32 and 43 have been canceled. Independent claims 1 and 31 and dependent claims 3-6, 8, 9, 14-17, 33-36, 41, 42, 46 and 47 have been amended. New independent claims 60-63 have been added

The claims before the Examiner are directed toward a network adapter, such as a host channel adapter (HCA), and a method of its use. The network adapter includes a host interface, an outgoing packet generator, an incoming packet processor, a network output port and a network input port. The host interface couples the network interface adapter to a host processor. The network output port transmits, via a network, outgoing request packets to remote responders and outgoing response packets to remote requesters. The network input port receives, via the network, incoming response packets from remote responders and incoming request packets from remote requesters. The incoming packet processor receives and processes both incoming response packets and incoming request packets. The outgoing packet generator generates outgoing request packets as requested by the host processor and also generates outgoing response packets in response to incoming request packets.

The outgoing packet generator includes a gather engine that gathers, from a system memory accessible via the host interface, and via a common data flow path,

both write data for outgoing request packets and read data for outgoing response packets. The incoming packet processor includes a scatter engine that scatters, to the system memory and via a common data flow path, read data from incoming response packets and write data from incoming request packets.

§ 112, Second Paragraph Rejections

The Examiner has rejected claims 5, 6, 9, 16 and 17 under § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

More generally, the Examiner has questioned the antecedent basis generally of terms used in the claims. Applicant's representative has reviewed the claims carefully and has determined that, for the most part, all the terms used in the claims in fact do have antecedent basis. In particular, the terms cited by the Examiner in claims 5, 6, 9, 16 and 17 as lacking antecedent basis have antecedent basis as follows:

"The queues" and "the schedule queues" of claim 5 have antecedent basis in "a plurality of schedule queues" in claim 4.

"The instances" of claim 5 has antecedent basis in "a plurality of transport service instances" earlier in claim 5.

"The instances" of claim 6 has antecedent basis in "a plurality of transport service instances" in claim 5.

"The queues" of claim 6 has antecedent basis in "a plurality of schedule queues" in claim 4.

"The execution engines" of claim 6 has antecedent basis in "one or more execution engines" earlier in claim 6.

"The queues" of claim 9 has antecedent basis in "a plurality of schedule queues" in claim 4.

In claim 16, it is clear that "a sequence of such packets" refers back to the type of packet most recently mentioned, *i.e.*, the outgoing response packet. Claim 16 has been amended to make this point explicit.

"The plurality of the instances: in claim 17 has antecedent basis in "a plurality of transport service instances" earlier in claim 17.

The review of the claims disclosed four cases of lack of antecedent basis. All four cases were inadvertent typographical errors that now have been corrected as follows:

In claim 1, "output packet" has been corrected to "outgoing packet".

In new claim 60, that is claim 13 rewritten in independent form and including an additional limitation as described below, "patents" has been corrected to "packets".

In claims 41 and 42, "the outgoing read response" has been corrected "the outgoing read response packet".

In addition, some of the claims have been amended as follows to make it easier to see the antecedent basis of the various terms.

In claim 4, "the queues" has been amended to "the schedule queues".

In claim 5, "the queues" has been amended to "the schedule queues" and "the instances" has been amended to "the transport service instances".

In claim 6, "the queues" has been amended to "the schedule queues" and "the instances" has been amended to "the transport service instances".

In claim 8, "the queues" has been amended to "the schedule queues".

In claim 9, "a write request packet" has been amended to "an incoming write request packet".

In claim 14, "the awaited packet" has been amended to "the awaited incoming response packet".

In claim 15, "the read request packet" has been amended to "the incoming read request packet".

In claim 17, "the instances" has been amended to "the transport service instances".

In claim 34, "the queues" has been amended to "the schedule queues".

In claim 35, "the instances" has been amended to "the transport service instances" and "the queues" has been amended to "the schedule queues".

In claim 36, "the queues" has been amended to "the schedule queues".

In claim 41, "the work item" has been amended to "the read response work item".

In claim 42, "the work item" has been amended to "the read response work item".

Claim 46 has been amended in the same manner as claim 16.

In claim 47, "the packets" has been amended to "the incoming read request packets" and "the instances" has been amended to "the transport service instances".

§ 102(e) Rejections – Pettey et al. '712

The Examiner has rejected claims 1, 4, 5, 7, 9, 10, 12, 14-19, 31, 34, 35, 37, 38, 40, 42 and 44-49 under § 102(e) as being anticipated by Pettey et al., US Patent No. 6,594,712 (henceforth, "Pettey et al. '712"). The Examiner's rejection is respectfully traversed.

As discussed below, independent claims 1 and 31 have been amended in a manner that places these claims in condition for allowance. It follows that claims 4, 5, 7, 9, 10, 12, 14-19, 34, 35, 37, 38, 40, 42 and 44-49 that depend therefrom also are allowable.

§ 103(a) Rejections – Pettey et al. '712 in view of Collins et al. '001

The Examiner has rejected claims 8 and 39 under § 103(a) as being obvious over Pettey et al. '712 in view of Collins et al., US Patent Application Publication No. 2002/0144001. The Examiner's rejection is respectfully traversed.

As discussed below, independent claims 1 and 31 have been amended in a manner that places these claims in condition for allowance. It follows that claims 8 and 39 that depend therefrom also are allowable.

§ 103(a) Rejections – Pettey et al. '712

The Examiner has rejected claims 11 and 41 under § 103(a) as being obvious over Pettey et al. '712. The Examiner's rejection is respectfully traversed.

As discussed below, independent claims 1 and 31 have been amended in a manner that places these claims in condition for allowance. It follows that claims 11 and 41 that depend therefrom also are allowable.

§ 103(a) Rejections – Pettey et al. '712 in view of Gasbarro et al. '004

The Examiner has rejected claims 2, 3, 6, 13, 32, 33, 36 and 43 under § 103(a) as being obvious over Pettey et al. '712 in view of Gasbarro et al., US Patent No. 6,948,004 (henceforth, "Gasbarro et al. '004). The Examiner's rejection is respectfully traversed.

Claims 2, 13, 32 and 43 have been canceled, thereby rendering moot the Examiner's rejection of these claims.

Gasbarro et al. '004 are cited by the Examiner only to show that gathering read and write data from system memory is taught in the prior art. Therefore, the present discussion focuses on Pettey et al. '712.

Pettey et al. '712 teach an InfiniBand target channel adapter (TCA) **202** of an InfiniBand I/O unit **108**. The overall structure of TCA **202** is illustrated in Figure 3. TCA **202** includes a transaction switch **302**, a bus router **306**, IB MACs **308** and PCI bus interfaces **312** and **316**. Bus router **306** performs InfiniBand transport layer operations. IB MACs **308** are the interfaces between TCA **202** and an InfiniBand fabric **114**. PCI bus interfaces **312** and **316** are the interfaces between TCA **302** and a host of TCA **302**. Transaction switch **302** directs packets, datagrams and command messages between IB MACs **308**, bus router **306** and PCI bus interfaces **312** and **316**. (Transaction switch **302** also includes packet memory blocks **304** in support of direct DRMA operations, which is the invention of Pettey et al. '712). The packets that TCA **202** can handle include the packets illustrated in Figures 10-13: SEND packets **1000**, RDMA write packets **1100**, RDMA read request packets **1200** and RDMA read response packets **1300**. It follows that the correspondences between components of the present invention, as recited in claims 1 and 31, and components of prior art TCA **302** are as in the following table:

Present invention	TCA **202**
Host interface	PCI bus interfaces **312** and **316**
Network output port	IB MAC **308**
Network input port	IB MAC **308**
Outgoing packet generator	Bus router **306**
Incoming packet processor	Bus router **306**

Figure 14 of Pettey et al. '712 is a block diagram of the logical structure of bus router **306**. Bus router **306** includes work queue management logic **1412** for processing InfiniBand work queue requests, transmit packet process logic **1414** for creating outgoing packets, receive packet process logic **1416** for processing incoming

packets and completion process logic for maintaining InfiniBand completion queues. Bus router **306** also includes a work queue memory **1402** in support of work queue management logic **1412**, a TxPP scratchpad memory in support of transmit packet process logic **1414** and a RxPP scratchpad memory in support of receive packet process logic **1416**.

Pettey et al. '712 are silent concerning the internal architecture of the various logics of bus router **306**. As best understood, the internal architecture of these logics is the same as the prior art structure described in the paragraph starting on page 3 line 22 of the specification of the above-identified patent application: a dual pipeline architecture with independent microprocessors and DMA engines for separate receive and transmit data paths.

By contrast, according to the present invention, as described in the specification on page 4 lines 19-23,

> ...a HCA is configured to handle both requester and responder communications flows using common hardware resources, rather than maintaining separate hardware paths for these functions as in devices known in the art.

There is neither a hint nor a suggestion of such an architecture in the prior art cited by the Examiner.

Therefore, to distinguish the present invention from the prior art cited by the Examiner with respect to data gathers, claims 1 and 31 have been amended to include the limitations of claims 2 and 32, respectively, and also the additional limitation that the gather engine gathers the write data (for the outgoing write request packet) and the read data (for the outgoing read response packet) via a common data flow path. Correspondingly, claims 2 and 32 have been canceled, claim 3 has been amended to depend directly from claim 1 and claim 33 has been amended to depend directly from

claim 31. Support for these amendment is found in the specification *inter alia* in Figure 2 and the description thereof on page 20 lines 8-19:

> An execution unit 60 queues the QPs having WQEs or quasi-WQEs that are awaiting service. A scheduler 64 selects the QPs to be serviced by arbitrating among the queues. The scheduling process is described in greater detail hereinbelow. A send data engine (SDE) 66 gathers the data to be sent from the locations in memory 38 specified by the WQEs, via TPT 58, and places the data in output packets for transmission over network 26. The data packets prepared by SDE 66 are passed to an output port 68, which performs data link operations and other necessary functions and sends the packets out over network 26. (emphasis added)

Note that WQEs are posted by host 24 for outgoing request packets (page 19 lines 12-14) and that quasi-WQEs are posted by TCU for outgoing response packets (page 19 lines 27-31). Therefore, both data for outgoing request packets and data for outgoing response packets are gathered via a common data flow path that includes execution unit 60 and SDE 66.

In addition, to distinguish the present invention from the prior art cited by the Examiner with respect to data scatters, claims 13 and 43 have been rewritten in independent form, as new claims 60 and 61, and also including the limitation that the scatter engine scatters the read data (from the incoming read response packet) and the write data (from the incoming write request packet) via a common data flow path. Support for this limitation is found in the specification *inter alia* in the description of RDE 56 of Figure 2 on page 19 lines 2-7:

> The RDE serves as a scatter engine both for RDMA write and send requests received by HCA 22 from remote requesters (such as HCA 28, in FIG. 1) and for RDMA read responses returned to HCA 22 by remote responders (HCA 28 or TCA 32, for example).

In other words, both data from incoming request packets and data from incoming response packets are scattered via a common data flow path that includes RDE 56.

With independent claims 1 and 31 allowable in their present form, it follows that claims 3, 6, 33 and 36 that depend therefrom also are allowable.

Other New Claims

New claims 62 and 63 also have been added.

New claim 62 recites the innovative aspect of the present invention with respect to a scatter engine of a network interface adapter. New claim 63 recites the innovative aspect of the present invention with respect to a gather engine of a network interface adapter. The support in the specification for new claims 62 and 63 includes the support cited above for the amendments to claims 1 and 31 and for new claims 59 and 60. Further support for new claims 62 and 63 is found in the specification on page 5 lines 27-32:

> The novel architecture of the present invention reduces markedly the amount of hardware required to implement the HCA, since the scatter and gather engines are shared by the requester and responder functions, rather than having a separate scatter and gather engine for each function as in devices known in the art.

Amendments to the Specification

The Examiner has objected to the specification for including an embedded hyperlink, at the end of the third paragraph on page 1. Applicant trusts that the fact, that the "amended' version of this paragraph that is submitted herewith is a hardcopy rather than a softcopy, overcomes the Examiner's objection.

The Examiner has required that the paragraph beginning on page 17 line 13 be amended to include references to published versions of the material that is included by reference. This paragraph now has been so amended. The first referenced patent application was published on November 7, 2002 as US Patent Application Publication No. 2002/0165899. The second referenced patent application was published on

December 6, 2001 as US Patent Application Publication No. 2001/0049755 and issued as US Patent No. 6,735,642 on May 11, 2004.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1, 31 and 60-63, and hence dependent claims 3-12, 14-19, 33-42 and 44-49 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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